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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/461,643	12/14/1999	KEITH DOW	10559/108001	4089

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FISH & RICHARDSON, PC
4350 LA JOLLA VILLAGE DRIVE
SUITE 500
SAN DIEGO, CA 92122

EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 01/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/461,643	Applicant(s) DOW, KEITH	
	Examiner Christopher E. Lee	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the request filed 13th of January, 2003 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/461,643, which the request is acceptable and an RCE has been established. Claims 1, 5, 6, 8, 10, 14, 16, 19 and 20 have been amended; no claim has been canceled; and no claim has been newly added. Currently, claims 1, 3-8, 10-14 and 16-22 are pending in this application.

Drawings

2. The corrected or substitute drawings were received on 10th of September, 2002. These drawings are acceptable.

Claim Objections

3. Claims 4 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

In the claims 4 and 5, all the subject matters are limited by their independent parent claim 1.

In the claims 11 and 12, all the subject matters are limited by their independent parent claim 8.

In the claims 17 and 18, all the subject matters are limited by their independent parent claim 14.

4. Claim 14 is objected to because of the following informalities: In the claim, the limitation "forming at least two parallel layers on a surface of a circuit board, with first and second signal lines on a selected layer of the board" doesn't make sense to one of ordinary skill in the art of PCB technologies because the multiple layers for routing signals, which is disclosed by the Applicant, cannot be implemented on a surface of a circuit board. Instead, the multiple layers are implemented in parallel to the surface of the circuit board. Therefore, the limitation would be considered as --forming at least two

parallel layers to a surface of a circuit board, with first and second signal lines on a selected layer of the board-- by the Examiner for the purpose of the claim rejection. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 3, 7, 8, 10, 14, 16 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al. [US 6,061,263 A; hereinafter Boaz] in view of Kumakura et al. [US 6,114,751 A; hereinafter Kumakura], Applicant Admitted Prior Art [hereinafter AAPA] and Perino et al.[US 6,160,716 A; hereinafter Perino].

Referring to claim 1, Boaz discloses a computer system (Fig. 1) comprising: processor (microprocessor 12); a memory unit (Rambus memory chip 21) configured to store data used by said processor (i.e., as system memory 64); a memory control unit (memory controller 15) configured to manage data flowing into and out of said memory unit (i.e., being coupled with said memory unit); a circuit board (RIMM PCB-Rambus In-line Memory Module Printed Circuit Board 17 of Fig. 1) comprising: <u>at least two layers (i.e., layer 16 of Fig. 2, layer 22 of Fig. 3, layer 38 of Fig. 4 and layer 40 of Fig. 5; See col. 2, line 40 and col. 3, lines 62-64) formed in parallel (i.e., spaced by a dielectric material; See col. 2, lines 59-61) to a surface (i.e., a surface of in-line memory module 14 of Fig. 2) of said circuit board (i.e., RIMM PCB-Rambus In-line Memory Module Printed Circuit Board),</u> a first signal line (i.e., signal lines from edge contact 18 of Fig. 3 to a Rambus memory chip 21 of Fig. 1), formed on a first layer (Fig. 3) of said circuit board and connected (See Fig. 1-3, col. 2, lines 27-65) between a first connection (i.e., a connection point of a route 24 and a pin of said Rambus memory chip 21 in Fig. 3) on said memory unit and said memory control unit (See col. 2, lines 29-30; i.e., wherein in fact that a plurality of in-line memory modules are coupled to a memory controller implies that said first signal line formed on said first layer of said circuit board connects between said first connection and said memory

control unit having signal lines on said mother board delivering its signals to said edge contact by way of said signal lines); and a second signal line (i.e., signal lines from said Rambus memory chip 21 to another Rambus memory chip 21 on said RIMM Circuit Board 17) also formed on said first layer of said circuit board and connected to said first connection (said connection point of said route 24 and said pin of said Rambus memory chip 21 in Fig. 3) on said memory unit, wherein said <u>first</u> layer defines a non-grounded gap between said first and second signal lines (See Fig. 3 and col. 4, lines 58-60; i.e., wherein in fact that the ground may be located in another layer implies said first layer defining a non-grounded gap between said first and second signal lines since its necessary ground lines are in another layer).

Boaz does not disclose a first portion of said second signal line substantially parallel to a first portion of said first signal line.

Kumakura discloses a printed circuit board with plural bus channel lines running in parallel with each other (Fig. 25-26), wherein a portion of a signal line substantially parallel (See col. 19, lines 42-47) to a portion of another signal line (See col.19, lines 35+; i.e., wherein in fact that the pitch of the bus channel lines is 0.25mm(10 mils) or 0.375mm(14.75 mils implies a portion of a signal line (i.e., a first bus channel line) substantially parallel to a portion of another signal line (i.e., a second bus channel line)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said parallel routing technique, as disclosed by Kumakura, to said circuit board routing, as disclosed by Boaz, for the advantage of reducing a routing congestion at said memory unit.

Boaz, as modified by Kumakura, does not teach a second portion of said second signal line at an acute angle relative to a second portion of said first signal line.

AAPA teaches a portion of a signal line at an acute angle relative to a portion of another signal line (See the angular relationship between the signal line 150,160 and the pin 155 in Fig. 2; Note the definition of the term "acute" in dictionary states -ending in a sharp point: as being or forming an angle measuring less than 90 degrees-, Merriam Webster's Colligiate Dictionary by Merriam-Webster, Inc.").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said acute angle routing technique, as disclosed by AAPA, to said circuit board routing, as disclosed by Boaz, as modified by Kumakura, for the advantage of minimizing an inductive cross-talk noise (See Kumakura, col. 14, line 59 through col. 15, line 9).

Boaz, as modified by Kumakura and AAPA, does not teach the widths of said lines and the distance separating said lines are each substantially equal.

Perino teaches the widths of lines (i.e., signal traces) on a circuit board is determined based on the impedance to be matched (See col.5, lines 48-49). And, the dielectric thickness of said circuit board layer for both of said signal lines are same because both of them are on said first layer. Furthermore, the distance spacing is also affecting the value of line impedance (See col.5, lines 37-41). Accordingly, Perino shows that the widths of lines (i.e., signal traces) and the distance separating said lines are each substantially equal (See Fig. 8, Example B as a prior art) in order to match the impedance (See col.5, lines 33-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by Boaz, as modified by Kumakura and AAPA, so that (1) the signal line widths of said first and second signal lines are equal because the determined impedance values should be same, and (2) said portion of said signal lines has set the separating distance equal to said width, for the advantage of (1) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32), and (2) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 3, Boaz discloses third and fourth signal lines (i.e., signal routes on the layer in Fig. 4), on a second layer of said circuit board, different than said first layer (See col. 2, lines 6-9, Fig. 3 and Fig. 4).

Referring to claim 7, Boaz et al. disclose said memory unit (Rambus memory chip 21) is a Rambus device.

Referring to claim 8, the method steps of claim 8 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 8.

Referring to claim 10, the method steps of claim 10 are inherently performed by the apparatus of claim 3, and therefore the rejection of claim 3 applies to claim 10.

Referring to claim 14, the method steps of claim 14 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 14.

Referring to claim 20, Boaz discloses a circuit board (RIMM PCB-Rambus In-line Memory Module Printed Circuit Board 17 of Fig. 1) comprising <u>at least two layers (i.e., layer 16 of Fig. 2, layer 22 of Fig. 3, layer 38 of Fig. 4 and layer 40 of Fig. 5; See col. 2, line 40 and col. 3, lines 62-64) formed in parallel (i.e., spaced by a dielectric material; See col. 2, lines 59-61) to a surface (i.e., a surface of in-line memory module 14 of Fig. 2) of said circuit board (i.e., RIMM PCB-Rambus In-line Memory Module Printed Circuit Board)</u> for use in a computer system (Fig. 1) comprising: a memory unit (Rambus memory chip 21); a memory control unit (memory controller 15); and a data bus (i.e., signal lines between memory control unit 15 and Rambus memory chip 21 in Fig. 1) connecting said memory control unit to said memory unit (See Fig. 1 and col. 2, lines 29-30) and comprising: a first signal line (i.e., signal lines from edge contact 18 of Fig. 3 to a Rambus memory chip 21 of Fig. 1),

formed on a first layer (Fig. 3) of said circuit board and connected to said memory control unit (See Fig. 1-3 and col. 2, lines 29-30; i.e., wherein in fact that a plurality of in-line memory modules are coupled to a memory controller implies that said first signal line formed on said first layer of said circuit board connects between said first connection and said memory control unit having signal lines on said mother board delivering its signals to said edge contact by way of said signal lines) and to a first connection on said memory unit (i.e., a connection point of a route 24 and a pin of said Rambus memory

chip 21 in Fig. 3); and a second signal line (i.e., signal lines from said Rambus memory chip 21 to another Rambus memory chip 21 on said RIMM Circuit Board 17) formed on said first layer of said circuit board and also connected to said first connection (said connection point of said route 24 and said pin of said Rambus memory chip 21 in Fig. 3) on said memory unit, wherein said first layer defines a non-grounded gap between said first and second lines (See Fig. 3 and col. 4, lines 58-60; i.e., wherein in fact that the ground may be located in another layer implies said first layer defining a non-grounded gap between said first and second signal lines since its necessary ground lines are in another layer).

Boaz does not disclose a first portion of said second signal line substantially parallel to a first portion of said first signal line.

Kumakura discloses a printed circuit board with plural bus channel lines running in parallel with each other (Fig. 25-26), wherein a portion of a signal line substantially parallel (See col. 19, lines 42-47) to a portion of another signal line (See col.19, lines 35+; i.e., wherein in fact that the pitch of the bus channel lines is 0.25mm(10 mils) or 0.375mm(14.75 mils implies a portion of a signal line (i.e., a first bus channel line) substantially parallel to a portion of another signal line (i.e., a second bus channel line)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said parallel routing technique, as disclosed by Kumakura, to said circuit board routing, as disclosed by Boaz, for the advantage of reducing a routing congestion at said memory unit.

Boaz, as modified by Kumakura, does not teach a second portion of said second signal line at an acute angle relative to a second portion of said first signal line.

AAPA teaches a portion of a signal line at an acute angle relative to a portion of another signal line (See the angular relationship between the signal line 150,160 and the pin 155 in Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said acute angle routing technique, as disclosed by AAPA, to said circuit board

routing, as disclosed by Boaz, as modified by Kumakura, for the advantage of minimizing an inductive cross-talk noise (See Kumakura, col. 14, line 59 through col. 15, line 9).

Boaz, as modified by Kumakura and AAPA, does not teach the widths of said lines and the distance separating said lines are each substantially equal.

Perino teaches the widths of lines (i.e., signal traces) on a circuit board is determined based on the impedance to be matched (See col.5, lines 48-49). And, the dielectric thickness of said circuit board layer for both of said signal lines are same because both of them are on said first layer. Furthermore, the distance spacing is also affecting the value of line impedance (See col.5, lines 37-41). Accordingly, Perino shows that the widths of lines (i.e., signal traces) and the distance separating said lines are each substantially equal (See Fig. 8, Example B as a prior art) in order to match the impedance (See col.5, lines 33-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by Boaz, as modified by Kumakura and AAPA, so that (1) the signal line widths of said first and second signal lines are equal because the determined impedance values should be same, and (2) said portion of said signal lines has set the separating distance equal to said width, for the advantage of (1) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32), and (2) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 21, Boaz discloses said first connection comprises a pin connection (i.e., a connection point of a route 24 and a pin of said Rambus memory chip 21 in Fig. 3).

Referring to claim 22, Boaz discloses said first connection on said memory unit comprises a pin connection (i.e., a connection point of a route 24 and a pin of said Rambus memory chip 21 in Fig. 3).

7. Claims 6, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz [US 6,061,263 A] in view of Kumakura [US 6,114,751 A], AAPA and Perino [US 6,160,716 A] as applied to claims 1, 3, 7, 8, 10, 14, 16 and 20-22 above, and further in view of Holman et al.[US 6,005,776 A; hereinafter Holman].

Referring to claim 6, Boaz, as modified by Kumakura, AAPA and Perino, discloses all the limitations of claim 6 except that does not teach said signal lines and said separate distance between them are each <u>substantially equal to</u> 5 mils.

Holman teaches that PCB technology may include conventional "5/5 routing rules" (See col. 3 lines 60-62) which requires 5 mils spacing between each transmission line and neighboring connection leads. Also, Holman discloses an example which shows 5 mil spacing and 5 mil width of transmission line (See Fig. 4, col.4, lines 15-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the 5 mils line width and spacing, as disclosed by Holman, to said circuit board routing, as disclosed by Boaz, as modified by Kumakura, AAPA and Perino, so that said widths of said lines and said distance separating said lines are set each substantially equal to 5 mils, for the advantage of providing a sufficient space between neighboring connection in general (See col. 4, lines 15-25).

Referring to claim 13, the method steps of claim 13 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 13.

Referring to claim 19, the method steps of claim 19 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 19.

Furthermore, the claims 6, 13 and 19 recite the subject matter "said signal lines are substantially equal to 5 mils on said circuit board" without any patentable advantage in the specification (See the claims 6, 13 and 19 and amended specification (filed on 14th of August, 2002) page 2, lines 8-20).

Therefore, the limitation of said signal lines are substantially equal to 5 mils on said circuit board in the claims 6, 13 and 19 is not patentably significant since it at most relates to the width of the signal line on said circuit board under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141*

Response to Arguments

8. Applicant's Response/Amendment filed on 13th of January, 2003 does not have any arguments.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/ CEL
January 21, 2003

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100